

Implementation of Automated Fault Isolation Test Programs for Maximum Likelihood Convolutional Decoder (MCD) Maintenance

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This article describes the automated fault isolation test programs that have been developed to support rapid turn-around factory (or depot) level maintenance of the Maximum Likelihood Convolutional Decoder (MCD). Functional requirements and detailed design characteristics are described, along with a summary of the evaluation and testing completed so far.

I. Introduction

Test programs, run on a computerized Logic Card tester, have been developed to support rapid turn-around factory (or depot) level maintenance for the MCD, which is currently being installed throughout the DSN as a part of the Telemetry Subsystem. The MCD requirements and design characteristics are described in a previous DSN Report (Ref. 1).

These programs were entirely developed based on the use of existing design test equipment and support software in order to realize maximum economy with minimum development time, and at the same time achieve excellent overall fault isolation capability and extensive computer generated documentation.

One program for each of the two MCD plug-in circuit cards has been developed. In size and complexity, the MCD Interface Board contains 59 Integrated Circuits (IC's) while the Decoder Board contains 92 IC's.

These programs were developed specifically to support a guaranteed maximum repair time of 30 calendar days, at the

repair facility, regardless of the nature or extent of the failure (excepting, of course, unforeseen catastrophic cases where a whole circuit board would have to be replaced). Also, a condition was added that if the expected repair effort, to be accomplished on a "time-and-material" cost basis, exceeded a predetermined threshold level, then the 30 day maximum period was to begin after receiving formal authorization to proceed with the repair effort from JPL.

In acceptance testing, the Interface Board program correctly identified 92% of the random customer selected faults manually inserted, while the Decoder Board program correctly identified 98% of the faults inserted (50 faults per board).

II. Specific Functional Requirements

The definition of the required performance characteristics for these programs is contained in the JPL Technical Requirements Document (Ref. 2).

The salient functional requirements, and the factors used in their selection, are discussed briefly below.

A. Logic Tester

The Mirco Model 530 Tester was selected as the test unit to be used for the following reasons:

- (1) Readily available (a standard catalog item).
- (2) Reasonable cost.
- (3) Rapid processing speed (200 KHz. Instruction rate).
- (4) Ease of Maintenance and Operation.
- (5) Availability of powerful support software, i.e., the FLASH (Fault Location And Simulation Hybrid) Simulator (Ref. 6), which offers greatly reduced programming time, improved testing comprehensiveness, and also provides computer generated program documentation.

B. Fault Isolation Capability

Each test program was required to be capable of identifying a circuit fault to within one IC (as a design goal) but in any event to within a group of not more than ten IC's, as an upper limit design goal.

The TRD also specified that, of the total number of faults simulated by FLASH (which includes shorts, opens, grounds, etc. for all circuit nodes on the board) at least 85% shall be correctly identified by each program.

Furthermore, all undetected (or incorrectly identified) faults were required to be isolatable using the available manual procedures called "Scope Trace" and/or "Time-Nodal-Test" transition counting.

C. Program Acceptance Test Procedure (PATP)

A specific PATP was required for each program. These procedures each contained a requirement that fifty (50) random customer selected faults (grounds) be inserted on each known good board, one fault at a time, and the test programs should correctly identify at least 85% of these known faults.

III. Design Approach

The basic approach used for this development effort was selected based on an awareness of commonly used digital test techniques and test equipment, including various types of test stimuli generation (pseudo-random, manually generated, etc.).

The utilization of FLASH was selected because of its ability to methodically and rapidly simulate all possible

faults, of all types, by use of its software modeling capability. This was considered to be far more complete, and economical, than other approaches involving more conventional manual techniques, of test stimuli generation and hardware testing (destructive and non-destructive).

Additionally, FLASH offered the advantages of reduced development time and effort, since it was fully developed and checked out, and had been successfully used on several previous test program developments of a similar type. FLASH offered the most complete and effective approach known, it was felt, because in addition to the primary automated mode of operation, it provided the data necessary for the two manual back-up modes called SCOPE TRACE and Time-Nodal-Test (TNT) Counts. By use of these back-up modes, fully non-ambiguous fault isolation can be achieved, involving minimal time, effort and operator skill.

IV. Design Description

A brief description of the Tester hardware and of the test software development, documentation and utilization is presented below. Detailed descriptions covering these subjects are provided in Refs. 3 through 10. The Tester and the test software are designed to evaluate circuit boards which contain all digital (i.e. 2-level) circuit devices.

A. Tester Description

The Tester used is the Mirco Model 530. This unit is portable, totally self-contained, includes all operator controls and displays on its top surface, and the boards to be tested mount directly to it via customized Interface Adaptor connection units, one for each of the two board types to be tested and one to be used with the Tester itself in its Self-Test mode.

The physical characteristics for this unit are listed below.

- (1) Input Power – 270 Watts (115 V.A.C., 60 Hz)
- (2) Size – 22.86 cm high
58.42 cm wide
40.64 cm deep
- (3) Weight – 24.9 kilograms
- (4) Operating Environment – 10°C (50°F) to 49°C (120°F), with 10 – 90% relative humidity.
- (5) Operator Panel – See Figure 1 (for more detail, see Ref. 8).

The Tester contains a microprogrammed test processor to execute the stored test program and to monitor and evaluate the test results. The processor instructions are implemented

using a combination of hardware and microcode, which provides for fast execution speed and the desired degree of flexibility.

The following basic modules are contained within the Tester:

- (1) Memory – Random access, 8K bytes (8 bits/byte)
- (2) Central Processor – Microprogrammed control.
- (3) Driver/Sensor Modules (3) – Each contain 32 lines which can be used as inputs to/or outputs from the board under test, under program control. Connections to the board are made via the board connector and also via eight (8) chip-clips which attach directly to specified IC's on the board.
- (4) Paper Tape Reader (Optical and Interface) – Used for program loading to the tester. Speed – 130 bytes/second.
- (5) Interface Adaptors (3) – Cable interconnection panels containing all unique wiring and cabling, including chip-clip connector cables which attach directly to specified IC's on the boards, one for each board and one for Tester Self-Test.
- (6) TNT (Transition Node Time) Probe and Processor – A probe which can be used to count the level changes that occur, at any circuit node, while the test program is run, and the result is displayed on the Tester. The result, or TNT signature, is a function of total changes in each direction.

B. Test Program Development

The test programs were developed based on full use of the capabilities provided by the FLASH support software, which was contractor developed and owned. These programs include NETGEN, MBUILD, FLASH, MSCOPE, DICT, MRPOST, and MCODE, each providing a specific function in the program development cycle. All support software is resident on a General Automation SPC-16 host computer (see Figure 2).

Initially, the programmer analyzed the logic design of the circuit board to be tested to become aware of all of its functional operating characteristics. He then developed a set of input stimuli patterns which are the series of tests that are incorporated into the final test program. For each test, a set of stimuli were provided as inputs to the board and the corresponding board outputs were monitored, all under program control. The input test patterns were extensive enough to drive all circuit nodes high and low one or more times during the test program.

The programmer provided information about each board that was used to develop a computerized model of the board. Inputs included an input/output pin assignment list, a device (IC) assignment list (IC's listed by standard type number) and an IC interconnection list. FLASH included a sub-routine library containing a subroutine model for each different IC type used. From these lists, NETGEN was used to create a logic image file of the board, and this file was in turn used by MBUILD to create a computer IMAGE of the board.

The programmer generated input stimuli patterns and the board IMAGE were used as inputs to FLASH, which also contains a simulator (or model) of the actual Model 530 Tester, and simulation runs were made using these three components. A sub-program within FLASH, called AUTO FAULT, automatically inserted all possible faults (opens, shorts, grounds, and incorrect timing delays to simulate faulty one-shots, etc.) into the board IMAGE, one at a time, and the test sequence was run until the fault was detected and an identifying entry, or fault signature, was stored. Faults not detected were stored in a No-Find list. In response to the stimuli contained within each test, another sub-program called SCOPE FILE monitors and records the state of all the circuit output nodes in the board image, at the end of each test in the test program. These data were used by MSCOPE to generate the SCOPE TRACE section of the documentation.

The DICT program sorted, tabulated and outputted all of the fault signature data (mentioned above) to generate the Fault Dictionary section of the documentation. Entries in this Dictionary are tabulated by test number and light numbers, which correspond to numbered lights on the Tester. When a fault is detected by the Tester, it shows the test number and one (or more) light numbers, and the corresponding entry in the Dictionary shows the one (or more) probably defective IC's on the board.

The MRPOST and MCODE programs were used to generate the test program object code tape, which is loadable directly into the Tester.

The test programs were evaluated using known good boards, operating with the Tester, to verify that the simulation software developed and used is accurate and correctly models the actual hardware.

The documentation package for each program contains the following:

- (1) Fault Dictionary
- (2) Scope Trace

- (3) No-Find List
- (4) Source and Object Programs Listings
- (5) Interface Adaptor Wire List
- (6) TNT Counts – for all circuit nodes.
- (7) Statistics Summary Sheet (See Figures 3 and 4)

The Statistics sheet shows the comprehensiveness, or percentage of total faults found, and also the fault isolation achieved, or percentage of isolation to one, vs. two or more, IC's. As indicated, 93% comprehensiveness was achieved for the MCD Interface board and 94.9% for the Decoder board. Thus most faults (93 – 95%) will be detected on the first run of the test program. Run time is less than 0.2 second for each program. For resolving undetected faults, or for improving fault isolation (if needed), two approaches are available. One is to evaluate each fault in the No-Find list, and by searching the Scope-Trace table, find a test where the subject circuit node should have changed state, then monitor this node with a separate oscilloscope and probe to determine whether or not the node is changing as shown by the Scope Trace. The other approach is to use the TNT probe, with the Tester, to count transitions at various suspect circuit nodes, based on general knowledge of the board operation and on the known symptoms of the malfunctions. Correct counts have been tabulated for all circuit nodes for each board. Many nodes can be checked in a short time because total run time is so short. Each repaired MCD will be re-tested using the MCD Acceptance Test Procedure (Ref. 1) to verify operational readiness.

V. Testing and Evaluation

The testing done so far consists of the Program Acceptance Tests which were completed at the end of the development cycle. As indicated above, fifty random faults (grounds) per board were selected by the customer and inserted, one at a time, on each board and the appropriate

test program was run on the Tester, after the board had been mounted to the Tester via its Interface Adaptor.

- (1) Interface Board
46 of 50 faults were detected and correctly identified, giving an accuracy of 92%. Of the 4 remaining faults, 3 were detected as test failures by the program, but the program did not identify the actual location of the faults by IC number and pin number. The program failed to detect the other fault and showed a PASS condition.
- (2) Decoder Board
49 of 50 faults were detected and correctly identified, giving an accuracy of 98%. The one remaining fault was detected by the program, but not correctly identified to the actual location.

The back-up fault detection and isolation procedures using Scope Trace and TNT counting were not evaluated at the time of the Acceptance tests, but will be exercised and evaluated in the near future. These procedures will be used to verify the fault location, as indicated by the Fault Dictionary, following a normal run of the test program. In this way faults will be positively identified before any IC's are replaced.

Through Dec. 1977, there have been two MCD units repaired at the factory, using these programs, and their use was entirely satisfactory. Additional performance data will be accumulated as these programs continue to be used for MCD repairs, in supporting the 33 MCD units which have been delivered to the DSN, since the last delivery from the factory in April 1976.

VI. Conclusion

The entire development of these programs proceeded as initially planned, on schedule and within budget, and the final performance quality exceeded the fixed, and the design goal, requirements specified in the TRD.

References

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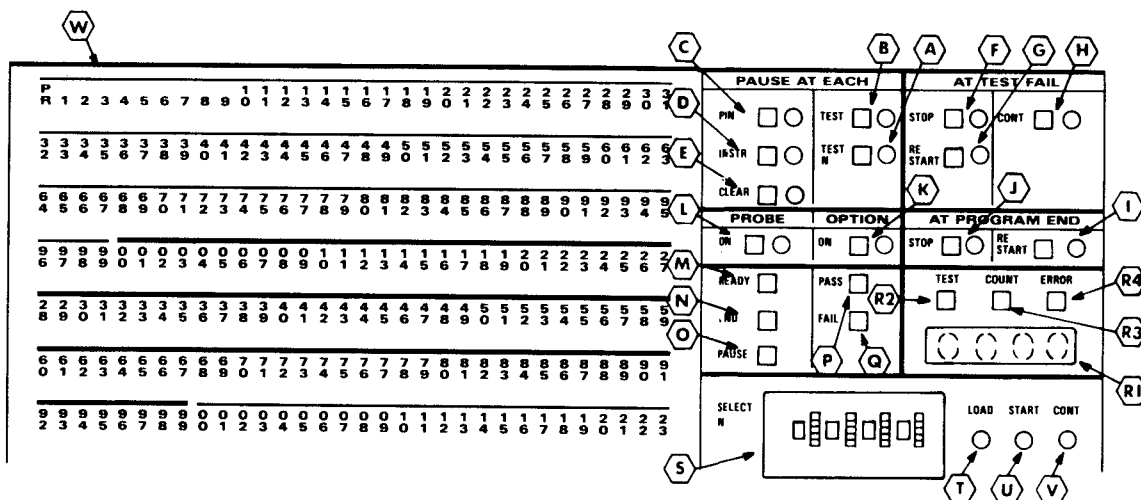
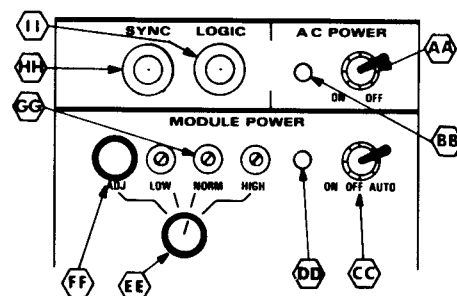
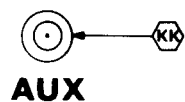
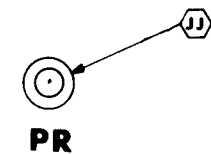


Fig. 1. Operator control test panel diagram

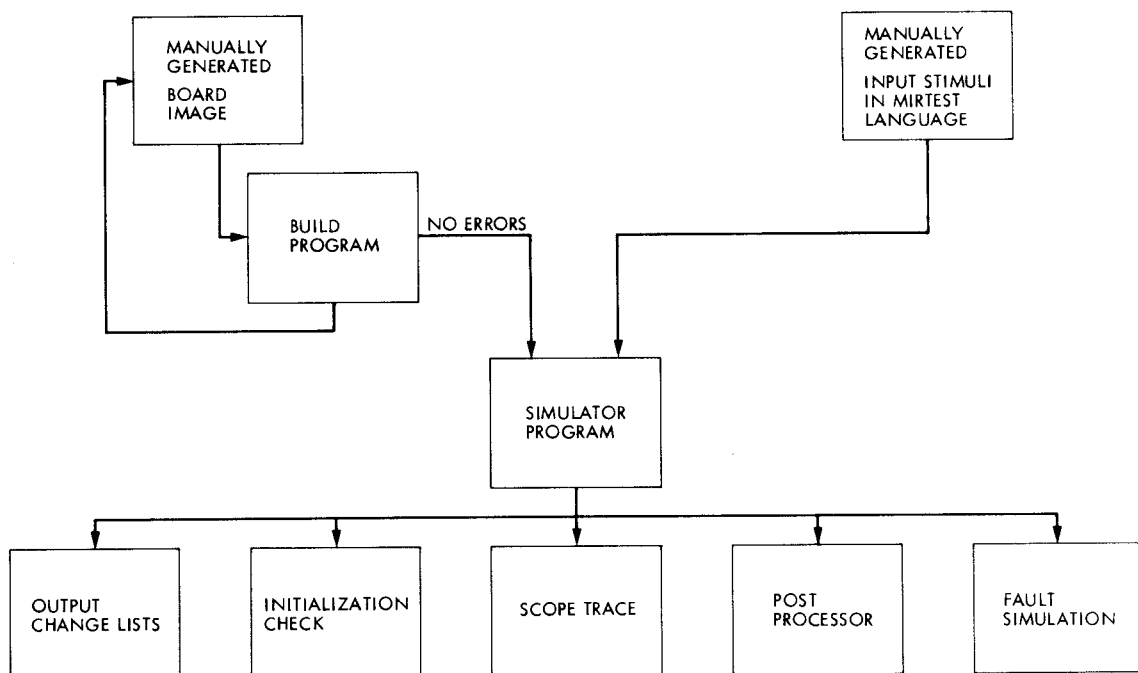


Fig. 2. Use of flash test generation software

TOTAL FAILURES - 1183
 FAILURES DETECTED - 1101
 COMPREHENSIVENESS - 93.0%

DICTIONARY DISTRIBUTION

CHIPS	PERCENTAGE OF DICTIONARY ENTRIES												
INDICATED	0%	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	75%	100%
	I....	I....	I....	I....	I....	I....	I....	I....	I....	I....	I....	I....	I....
1 CHIP.	***** 51.6%												
2 CHIPS	***** 26.0%												
3 CHIPS	***** 12.8%												
4 CHIPS	**** 04.1%												
5 CHIPS	*** 03.3%												
6 CHIPS	. 00.4%												
7 CHIPS	.* 00.8%												
8 CHIPS	.* 00.8%												
9 CHIPS	. 0%												
10 OR >	. 0%												

AVERAGE DICTIONARY ENTRY = 1.90 CHIPS

Fig. 3. MCD interface board program, statistic sheet UUT No. 3023

TOTAL FAILURES - 2300
 FAILURES DETECTED - 2184
 COMPREHENSIVENESS - 94.9%

DICTIONARY DISTRIBUTION

CHIPS	PERCENTAGE OF DICTIONARY ENTRIES												
INDICATED	0%	5%	10%	15%	20%	25%	30%	35%	40%	45%	50%	75%	100%
	I.....	I.....	I.....	I.....	I.....	I.....	I.....	I.....	I.....	I.....	I.....	I.....	I.....
1 CHIP	***** 65.0%												
2 CHIPS	***** 17.9%												
3 CHIPS	***** 03.6%												
4 CHIPS	***** 04.0%												
5 CHIPS	.* 01.4%												
6 CHIPS	.* 01.2%												
7 CHIPS	.* 01.0%												
8 CHIPS	. 00.2%												
9 CHIPS	. 00.2%												
10 OR >	. 00.2%												

AVERAGE DICTIONARY ENTRY = 1.70 CHIPS

Fig. 4. MCD decoder board program, statistic sheet UUT No. 6803